CLAIMS

Claim 1:

A hardware device for concurrently processing a plurality of tasks associated with an algorithm which includes a number of processes some of which are dependant on binary decisions, said device comprising:

a plurality of task units (10, 12 14) for processing data, making decisions and/or processing data and making decisions;

a task interconnection logic means (16) interconnecting the task units for communicating actions from a source task unit to a destination task unit.

each of said task units including a processor (18) for executing the steps of the associated task in response to a received request action; and,

a status manager (20) for handling actions from source task units and building actions to be sent to destination task units.

Claim 2.

Hardware device according to claim 1, wherein said actions communicated from a source task unit to a destination task unit are START used to activate the processor (18) of said destination task unit, KILL used to cancel the task associated with said destination task unit and VALID used to confirm that task associated with said destination task unit corresponds to a decision included in said task.

Claim 3.

Hardware device according to claim 2, wherein said status manager (20) activates said processor (18) for processing the steps of the task associated with said destination task unit when the action received from a source task unit is START.

Claim 4.

Hardware device according to claim 3, wherein said status manager (20) is a state machine.

Claim 5.

Hardware device according to claim 3, wherein each of said task units (10, 12, 14) further comprises a plurality of control/data registers (22, 24, 26) each corresponding, for the task associated with said task unit, to an instance of the algorithm flow, each one of said control/data registers comprising a control field composed of a completion bit(C) set to 1 when the associated task is completed, a validation bit (V) set to 1 when the associated task is validated and a L/R bit indicating that the output in the algorithm flow is left or right when said task includes a decision.

Claim 6.

Hardware device according to claim 5, wherein each of said control/data registers (22, 24, 26) includes a data field which is loaded if necessary by said status manager (20) activated by an action received from a source task unit, said processor (18) using these data for executing the task associated with said task unit and replacing them if necessary.

Claim 7.

Hardware device according to claim 6, wherein said completion bit (C) is sent by said

processor (18) to said status manager (20) after completion of the task execution.

Claim 8.

Hardware device according to claim 5, 6 or 7, wherein said control/data register (22, 24 or 26) corresponding to a specific instance is cleared by said status manager (20) when this one receives an action KILL for the task associated with said task unit and for said specific instance.

Claim 9.

Hardware device according to any one of claims 5 to 7, wherein each one of said task units (10, 12, 14) further comprises two configuration registers CONFIG.L (28) and CONFIG.R (30) which are respectively selected by the binary value of said bit L/R of the control/data register (22, 24, 26) of the instance being considered, the contents of said configuration registers being loaded at the beginning of the algorithm processing for defining the task to be activated, the action to be performed and the instance to be considered.

Claim 10.

Hardware device according to any one of claims 1 to 7, wherein said task interconnection logic block (16) is composed of three-state drivers (40, 42, 44) each one of said drivers being associated with one of said tasks as input task and a number of buses equal to the number of said tasks as output tasks, one of said buses being selected by the driver corresponding to an input task after decoding an action word by said driver.